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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,745	09/23/2003	David W. Boggs	884.942US1	1789

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EXAMINER	
DINH, TUAN T	
ART UNIT	PAPER NUMBER
2841	
MAIL DATE	DELIVERY MODE
10/07/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/668,745	BOGGS ET AL.	
	Examiner	Art Unit	
	Tuan T. Dinh	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15,17-20 and 28-33* is/are pending in the application.

4a) Of the above claim(s) *17-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,28-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Applicant's Appeal Brief is persuasive and, therefore, the finality of that action is withdrawn.

Note of claimed language:

Examiner is considered the term "***adapted to***" as well as defined as ***an intended use limitation***. The claim limitation, that employ phrases of the type "adapted to" is typical of claim limitation, which may not distinguish over prior art according to the principle. It has been held that the recitation that *an element is "adapted to" perform or is "capable of" performing a function is not a positive limitation* but only requires the ability to so perform, see In re Venezia, 189 USPQ 149 (CCPA 1976).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-9 and 28-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiraki (U.S. Patent 6,969,808) in view of Johnson et al. (U.S. Patent 6,469,530).

As to claims 1-5, 7-9, Shiraki discloses a device, which is a semiconductor chip or a multilayer circuit board (column 1, lines 16-17, claims 7-8) as shown in figures 1-4 comprising:

first and second major exterior surfaces (top and bottom surfaces of the board, see figure 2), at least one of the first and second major exterior surfaces including a plurality of component mounting pads (not label, but the pads are formed on the first surface of the multilayer circuit board);

a signal (31) carrying plated through hole (plated hole 21) terminating at the at least one the first or second major exterior surfaces; a pad (top and bottom portion of the plated 21) and the signal carrying connected to the pad, an ant-ipad (clearance hole formed between the ground layer and the pad) substantially surround the pad

a plane metallization layer, which is power, ground, or reference voltage planes (26-ground layer, 27-power layer, column 3, lines 35-36, claims 2-4) within the device surround the pad and anti-pad (see figure 9); and a plated through hole or via (41, column 3, line 41) attached to the plane metallization layer (26 or 27) and terminating at the at least one of the first and second major exterior surfaces including the plurality of component mounting pads, the plated through hole (41) electrically isolated from the plurality of component mounting pads, and a signal through hole (21) having a signal layer (11) passed through the plane metallization layer (26; 27) and terminated at the pad at the first surface (claim 5).

Shiraki does not specific disclose **a circuit tester** for determining if a current will flow between the pad and the via and the plane metallization to test the spacing of the

plane metallization layer from the signal through hole that passes through the plane metallization layer.

Johnson et al. teaches a method and apparatus for testing an IC package as shown in figure 3 comprising a tester (30) having probes (42) tested on pads (24) and through holes (34) of the PCB (12).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a teaching of Johnson et al. employed in the device of Shiraki in order to prevent an internal short circuit.

As to claim 6, Shiraki as modified by Johnson et al. discloses the signal (signal layer 11 connected to the through hole 21) carrying plated through hole (21), which passes though and electrically isolates the plane metallization layer (26; 27) and is connected to the pad at the first major exterior surface.

As to claims 28-33, Shiraki discloses a device (PCB) as shown in figures 1-4 comprising:

first and second major exterior surfaces (top and bottom surfaces of the board, see figure 2), at least one of the first and second major exterior surfaces including a plurality of component mounting pads (not label, but the pads are formed on the first surface of the multilayer circuit board);

a feature, which is a trace or signal layer (11) or a signal carrying through hole (21) positioned within the device;

a plane metallization layer (26-ground layer, 27-power layer, column 3, lines 35-36, claims 2-4) within the device; and a plated through hole (41, column 3, line 41)

attached to the plane metallization layer (26 or 27) and terminating at the at least one of the first and second major exterior surfaces including the plurality of component mounting pads, the plated through hole (41) electrically isolated from the pads, and the feature or signal layer (11) passed through and isolates the plane metallization layer (26; 27) and terminated at the pad at the first surface (claim 5).

Shiraki does not disclose *a test device for* testing the feature and the metallization layer.

Johnson et al. teaches a method and apparatus for testing an IC package as shown in figure 3 comprising a tester (30) having probes (42) tested on pads (24) and through holes (34) of the PCB (12).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a teaching of Johnson et al. employed in the device of Shiraki in order to prevent an internal short circuit.

3. Claims 10-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiraki ('808) in view of Conn et al. (U.S. Patent 5,418,690), and further in view of Johnson et al. ('530)

As to claims 10-15, Shiraki discloses a device, which is a semiconductor chip or a multilayer circuit board (column 1, lines 16-17, claims 11-12) as shown in figures 1-4 comprising:

first and second major exterior surfaces (top and bottom surfaces of the board, see figure 2), at least one of the first and second major exterior surfaces including a

plurality of component mounting pads (not label, but the pads are formed on the first surface of the multilayer circuit board);

a plane metallization layer, which is power, ground, or reference voltage planes (26-ground layer, 27-power layer, column 3, lines 35-36, claims 13-15) within the device; and

a plated through hole (41, column 3, line 41) attached to the plane metallization layer (26 or 27) and terminating at the at least one of the first and second major exterior surfaces including the plurality of component mounting pads, the plated through hole (41) electrically isolated from the plurality of component mounting pads, and a signal through hole (21) (a signal layer (11) connected to the through hole 21) passed through and spaced away the plane metallization layer (26; 27) and attached at the pad at the first surface (claim 5).

Shraki does not specific disclose a processor, a memory, and the device associated with at least one of the processor and memory.

Conn et al. shows a printed circuit board (PCB 10-figure 1 and 31-figure 4) comprising a processor (11) and a memory chip (12; 13) mounted on the PCB.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a teaching of Conn et al. employed in the device of Shiraki in order to provide a function as operator programs or applications and store data in a computer system.

Shiraki and Conn et al. do not disclose *a circuit test apparatus for testing* the spacing between the plane metallization layer and the pad associated with the signal through hole.

Johnson et al. teaches a method and apparatus for testing an IC package as shown in figure 3 comprising a tester (30) having probes (42) tested on pads (24) and through holes (34) of the PCB (12).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a teaching of Johnson et al. employed in the device of Shiraki and Conn et al. in order to prevent an internal short circuit.

Response to Arguments

Applicant's arguments with respect to claims 1-15, 28-33 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reichard Dean can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tuan T Dinh/
Primary Examiner, Art Unit 2841.